AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph number [0040] with the following amended version thereof.

[0040] In the embodiment, the access attempt proceeds essentially as represented by the high-level flow diagram of Fig. 3 and as described below. When on of the [[Ms]] MS stations needs to communicate, the MS selects an available preamble code sequence for one of the RACH sub-channels based on a random selection method, and then the MS transmits a random-access signal using the selected preamble code sequence. The random-access signal transmission consists of repeated preamble code sequence, preferably in orthogonal sequence, such as the modified Hadamard code sequence exclusive-or gated with the cell-site signature sequence with length of 64 chips. In a preferred embodiment shown in Fig. 4, the random-access signal may also consist of a data portion, comprising of a mobile station identification number (MS ID) field, a message field for carrying short messages (typically under 8 bytes) to the BS, and a cyclic-parity-check (CRC) code protecting the MS ID and the message. The data portion of the random-access signal is typically obtained by modulating the respective preamble sequence with the data bits using binary-phase-shift-keying (BPSK) type modulation. In this preferred embodiment, a guard period of 896 chips is appended at the end of the random-access signal. Each random-access signal is one slot length of the high-capacity channel, e.g. 250 μsec in length.

Please replace paragraph number [0056] with the following amended version thereof.

[0056] When a mobile station selects a preamble code for use in its access attempt, the preamble code is specific to only one of the RACH sub-channels, and the mobile station sends [[it]] its access signal using the selected sub-channel code as the preamble. However, the BS

constantly monitors the sub-channel transmissions and computes a CLPCS value for each of the available sub-channels. The BS periodically broadcasts the CLPCS value of each available sub-channel to the entire cell.

Please replace paragraph number [0083] with the following amended version thereof.

[0083] The signals from the MF banks 47 and 48 are supplied in parallel to a processor 49, which performs automatic frequency correction (AFC) and phase rotation, and the outputs thereof are processed through a rake combiner and decision/demapper circuit 51, to recover and re-map the chip sequence signals to the original data values. The data values for the I and Q channels also are multiplexed together to form a data stream at 56 Mbps. This detected data stream is applied to a deinterleaver 52. The deinterleaver 52 reverses the interleaving performed by interleaver element [[32]] 2 at the transmitter. A decoder 53 performs forward error correction on the stream output from the deinterleaver 52, to correct errors caused by the communication over the air-link and thus recover the original input data stream (at 28 Mbps). The receiver section also includes a clock recovery circuit 54, for controlling certain timing operations of the receiver, particularly the A/D conversions.